REMARKS/ARGUMENTS

In view of the foregoing amendments and the following remarks, reconsideration and allowance of this application is requested. Claims 1-2, 4-9, 15, 22-23 and 39 are now pending, with claim 1 being independent.

The Examiner rejected pending claims 1-2, 4-9, 15, 22-23 and 39 under 35 U.S.C. § 112, first paragraph as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The Examiner states that the specification, as originally filed, does not disclose "the semiconductor chip having a planar active surface including an integrated circuit protected by an inorganic overcoat with side walls", and "a planar outer surface covering the side walls of the inorganic overcoat", as recited in unamended claim 1.

In establishing the disclosure of an application, Applicants may rely on the originally filed specification, drawings, and claims as support for later amendments to the application (see MPEP 608.04, 608.01(l), 2163.01, 2163.03, 2163.05). The Examiner rejects claims 1-2, 4-9, 15, 22-23, and 39 because an inorganic overcoat with side walls and a planar outer surface covering the side walls of the inorganic overcoat is claimed and the specification, as originally filed, does not disclose these limitations. Applicants respectfully disagree.

Support is provided in Figure 2 and the "Detailed Description of the Preferred Embodiments" for the limitations recited in claim 1. Figure 2 is described on page 14, lines 20-31 and page 15, lines 1-16. Page 14 states:

> In the embodiment of FIG. 2, the contact pad has an added conductive layer 205 on the pad metallization 202. This layer 205 is conformal to the surface of the chip and provides a reliable, low resistance contact to the pad metallization 202, as well as a strong and reliable adhesion to the *inorganic overcoat 203*. As FIG. 2 shows, layer 205 covers not only the area of the pad 202a proper, but also the window *side walls* of protective layers 203 and a portion 205a of the surface surrounding the pad window. [Emphasis added]

The description of Figure 2 given on pages 14-15 provides sufficient disclosure so as to enable one skilled in the art to make and/or use the invention claimed in claim 1. Therefore, claims 1-2, 4-9, 15, 22-23 and 39 are sufficiently supported by the

specification to enable one skilled in the art to make and/or use the invention. Accordingly, Applicants respectfully request the Examiner withdraw this rejection.

Claim 1 has been amended in response to the Examiner's rejection under 35 U.S.C. §112, second paragraph.

As amended, claim 1 presents a semiconductor device that includes a semiconductor chip with a planar active surface. The planar active surface has an integrated circuit protected by an inorganic overcoat, the integrated circuit having metallization patterns with a plurality of contact pads. The inorganic overcoat includes side walls over each of the contact pad surfaces. As shown in Figure 2, each of the contact pads 202 has an added conductive layer 205 on the metallization patterns. The added conductive layer 205 has a conformal surface adjacent the semiconductor chip that includes peripheral portions 205a of the inorganic overcoat 203. The added conductive layer 205 also has a planar outer surface 206, 207 covering the side walls of the inorganic overcoat and defining a flat outline substantially parallel to the chip surface (surface of inorganic overcoat 203), the planar outer surface suitable to form metallurgical bonds without melting. As shown in Figure 3, a non-conductive adhesive layer 301 is over the inorganic overcoat 203.

Amended claim 2 recites that the adhesive layer fills the spaces between the added conductive layers on each of the contact pads. Claim 2 further recites that the adhesive layer is the same height as the conductive layers on each of the contact pads.

Claim 39 recites that the side walls of the inorganic overcoat are window side walls.

Independent claim 1 stands rejected under 35 U.S.C. § 102(b) as anticipated by Berndlmaier et al. (5,053,851). Applicants request reconsideration and withdrawal of this rejection for at least the reason that Berndlmaier does not describe or suggest a non-conductive adhesive layer over the inorganic overcoat as admitted by the Examiner in paragraph 9 of the Office Action.

Claim 2 stands rejected under 35 U.S.C. § 103(a) as obvious over Berndlmaier in view of Fan et al. (6,605,524). However, Fan fails to remedy the failure of Berndlmaier to describe or suggest a non-conductive adhesive layer over the inorganic overcoat. Fan describes in the Abstract and Figures 13 and 14 a process in which layers of Under Bump Metal (UBM) 18 and a layer of solder metal 28 are created and overlie a contact pad 12 after which a layer of polyimide

30 is deposited. In between contact pad 12 and seed layer 16 is a passivation layer 14 that is patterned, exposing contact pad 12. As described in column 8, lines 51-67 and column 9, lines 1-5, the thickness of the polyimide layer 30 can be controlled and selected to a desirable value in relation to the height of the column of solder material 28. The height over which the solder column 28 protrudes above the surface of the layer 30 can be controlled from which follows that the diameter of the solder ball shown in Figure 14 that is created by reflowing the solder column 28 can be controlled. The solder ball connects the semiconductor 10 containing integrated circuits to a wiring board. Fan does not describe or suggest a non-conductive adhesive layer over the inorganic overcoat passivation layer 14. In Fan, polyimide 30 covers passivation layer 14. Nowhere in Fan is polyimide 30 described as an adhesive layer. As described in column 7, lines 61-67 and column 8, lines 1-24 polyimides are used in the semiconductor art not for adhesion characteristics but as dielectrics that can tolerate temperatures of up to 500 degrees C. without degradation of their dielectric characteristics. Furthermore, as shown in Applicants' Figure 3 and described on page 20, lines 3-12 and Figure 6B as described on page 21, line 31 to page 22, line 2, non-conductive adhesive layer 301/630 has the same height 301a as the added conductive layers 200 over the contact pad. Applicants' adhesive layer 301/630 serves to fill the spaces between the added conductive layers on each of the contact pads to create a planar, flat surface for attachment to wiring board 620 (Figure 6B). The adhesive characteristic of the adhesive layer allows for strong attachment of the semiconductor chip to the wiring board. In Fan, as shown in Figures 13 and 14, polyimide layer 30 does not extend the full height of solder ball material 28 as the solder ball is used to connect the semiconductor chip to the wiring board and the polyimide layer 30 does not assist in attachment. Thus, there is no need for the polyimide layer 30 to be an adhesive layer and Fan does not describe or suggest a non-conductive adhesive layer over the inorganic overcoat passivation layer 14. Accordingly, Applicants request reconsideration and withdrawal of the rejection for at least the reasons discussed above and with respect to claim 1.

Fan also does not describe or suggest the limitation given in claim 2 wherein the adhesive layer is the same height as the conductive layers on each of said contact pads as described above. In no part of the Fan reference is non-conductive polyimide layer 30 described as the same

height as the conductive layer solder material 28. Thus, Applicants request reconsideration and withdrawal of the rejection of claim 2 for this further reason.

Claims 22 and 23 stand rejected under 35 U.S.C. § 103(a) as obvious over Berndlmaier in view of Elenius et al. (6,287,893). However, Elenius fails to remedy the failure of Berndlmaier to describe or suggest a non-conductive adhesive layer over an inorganic overcoat. Elenius describes, as shown in Figure 2, a chip scale package 8 for a flip chip integrated circuit 10 that includes a redistribution conductive layer 30 upon the upper surface of a semiconductor wafer 14 for simultaneously attaching to solder balls 28 as well as with the conductive bond pad 18 of the underlying integrated circuit. The redistribution conductive layer 30 is covered by a passivation layer 33 that may be formed of Benzocyclobutene, polyimides, polyolefins and other organic or inorganic passivations. No part of the Elenius reference describes or suggests a non-conductive adhesive layer over the inorganic passivation overcoat. Accordingly, Applicants request reconsideration and withdrawal of the rejection for at least the reasons discussed above and with respect to claim 1.

Independent claim 1 also stands rejected under 35 U.S.C. § 102(b) as anticipated by Camilletti et al. (5,693,565). Applicants request reconsideration and withdrawal of this rejection for at least the reason that Camilletti does not describe or suggest a non-conductive adhesive layer over the inorganic overcoat as admitted by the Examiner in paragraph 11 of the Office Action. Camilletti also does not describe or suggest that the added conductive layer has a planar outer surface covering the side walls of the inorganic overcoat and defining a flat outline substantially parallel to the chip surface.

Camilletti, in relevant part, as shown in Figure 4 and described in columns 3, 4, and 8 teaches a semiconductor chip 30A including a silicon substrate 10A with a front side surface 21A on which integrated circuits are formed. Contact pad 11A electrically connects the integrated circuits. A passivation layer 12A is an insulating layer over surface 21A and the side edges of contact pad 11A. An intermediate metal layer 15A is applied over the window opening of contact pad 11A. Intermediate metal layer 15A is used as a supporting surface for solder bump 16A which functions as a final electrical connection. Preceramic silicon-containing resin 17, followed by a silicon carbide ceramic layer 18 covers primary passivation layer 12A. As shown in Figure 4, Camilletti does not describe or suggest that the added conductive layers

(15A/16A) have a planar outer surface covering the side walls of the inorganic overcoat (12A) and defining a flat outline substantially parallel to the chip surface. In Camilletti, the added conductive layers covers the side walls of the inorganic overcoat opened over the surface of the contact pad and do not cover the opposite side walls over the side edges of the contact pad. Camilletti also does not describe or suggest that the added conductive layer has a planar outer surface defining a flat outline substantially parallel to the chip surface 21A. Conductive layers 15A/16A do not cover the bumps and ridges of passivation layer 12A, resin 17, and ceramic layer 18 and do not form a flat outline substantially parallel to the chip surface. In Camilletti, intermediate metal layer 15A, and solder bump 16A shown in Figure 4 would have to extend in both directions to cover the side walls of passivation layer/inorganic overcoat 12A, resin 17, and ceramic layer 18 to create a flat outline substantially parallel to the chip surface.

For at least the reasons given above, Applicants respectfully submit that claim 1 is patentable over Camilletti.

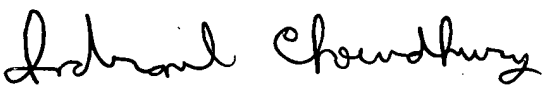
Claim 2 stands rejected under 35 U.S.C. § 103(a) as obvious over Camilletti in view of Fan et al. (6,605,524). However, as discussed above Fan fails to remedy the failure of Camilletti to describe or suggest a non-conductive adhesive layer over the inorganic overcoat. Accordingly, Applicants request reconsideration and withdrawal of the rejection for at least the reasons discussed above and with respect to claim 1.

Claims 22 and 23 stand rejected under 35 U.S.C. § 103(a) as obvious over Camilletti in view of Elenius et al. (6,287,893). However, as discussed above Elenius fails to remedy the failure of Camilletti to describe or suggest a non-conductive adhesive layer over an inorganic overcoat. Accordingly, Applicants request reconsideration and withdrawal of the rejection for at least the reasons discussed above and with respect to claim 1.

Claims 2, 4-9, 15, 22-23, and 39 depend from independent claim 1. Accordingly, Applicants request reconsideration and withdrawal of the rejections for claims 2, 4-9, 15, 22-23, and 39 for at least the reasons discussed above with respect to claim 1.

In view of these remarks and amendments, Applicants submit that this application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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